OMNITRONIC®

OMNITRONIC CDP-450

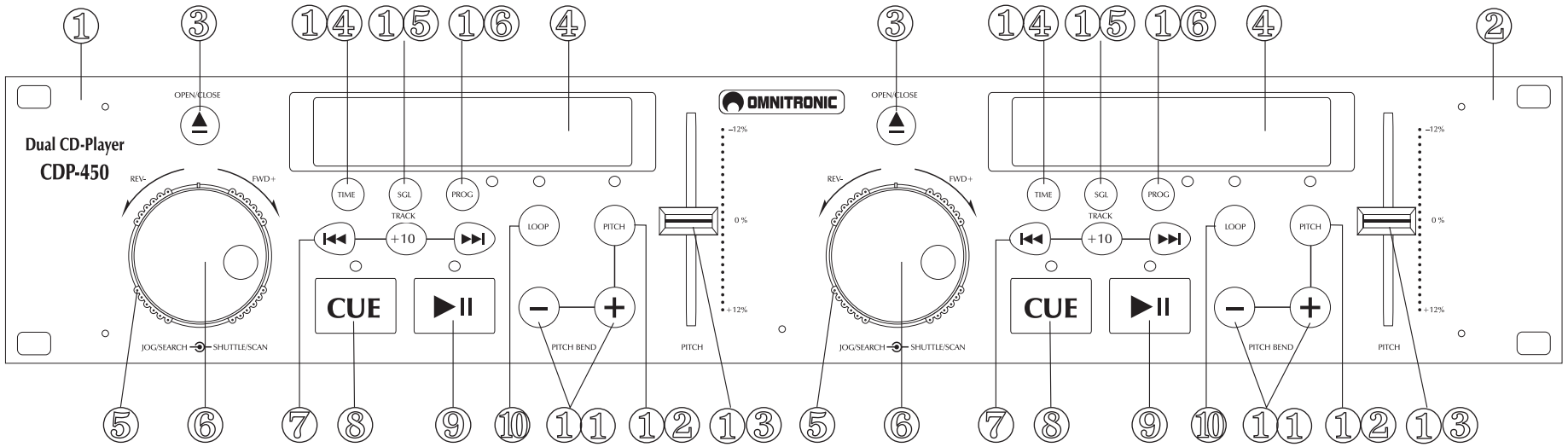
Dual-CD-Player

Classic-Edition
Design-Edition

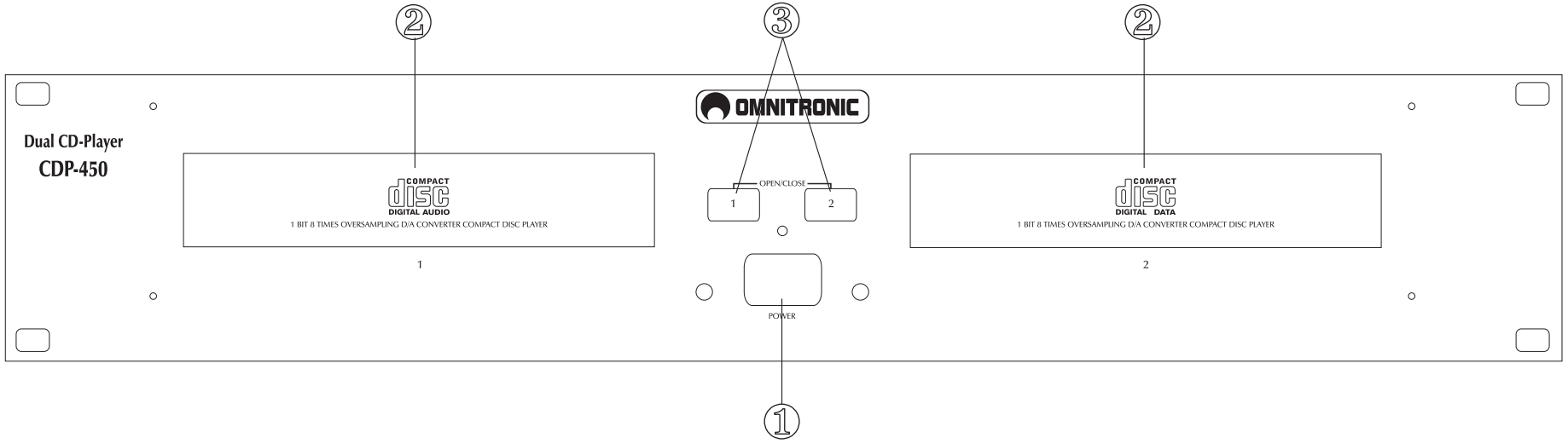
Service-manual
Serviceunterlagen
Documents techniques

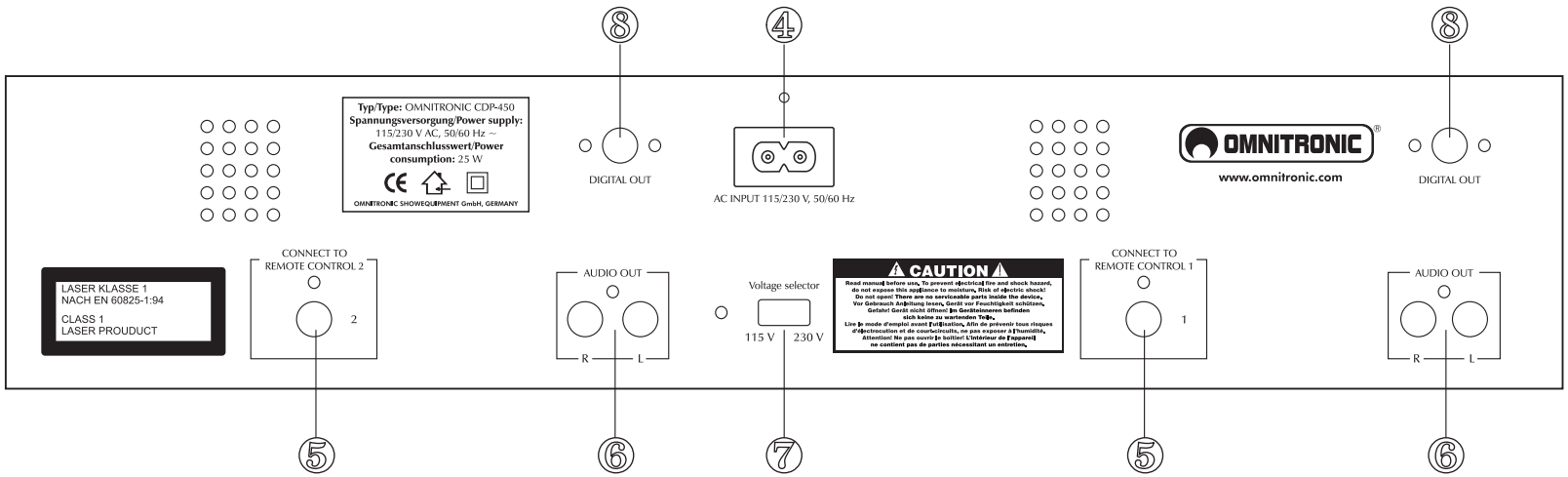
Version 2.0

Steuereinheit
Controller
Bloc de commande
Controlador



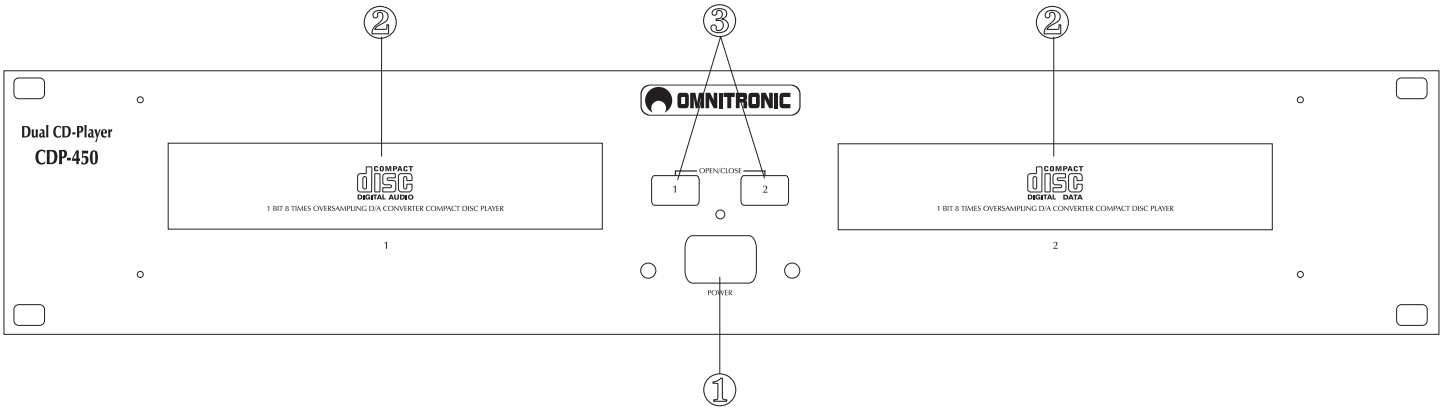
Doppel-CD-Player
Main unit
Bloc des lecteurs
Unidad principal





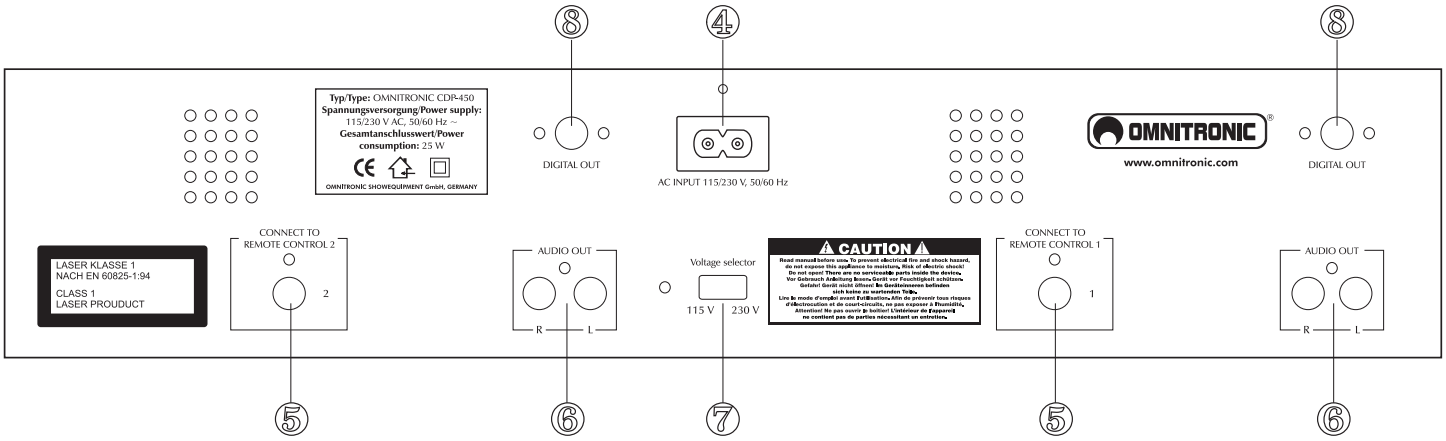
Main unit

Frontpanel:



1. POWER SWITCH
2. DISC-TRAY
3. OPEN/CLOSE BUTTON

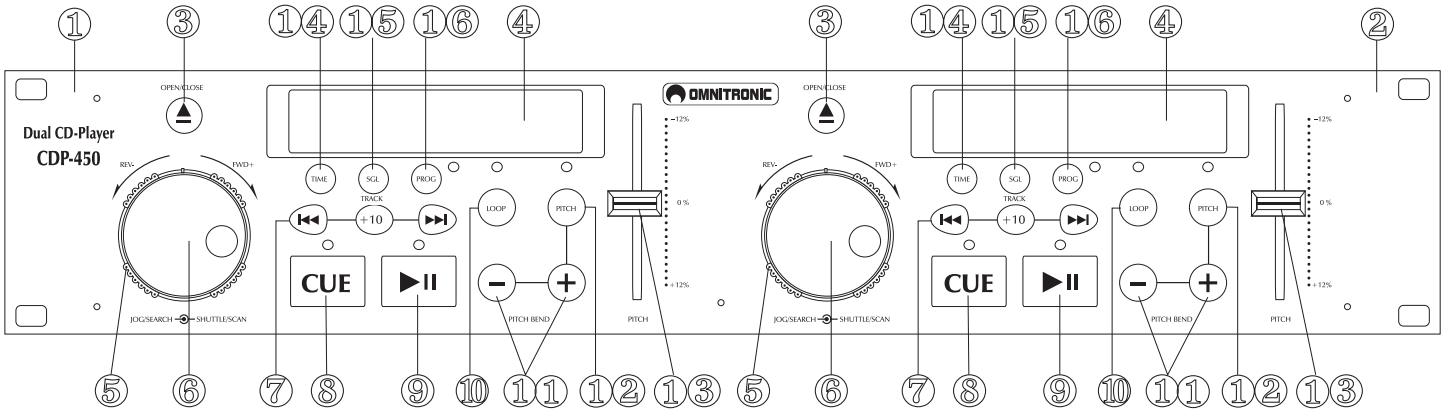
Rear panel:



4. AC CONNECTION
5. VOLTAGE SELECTOR
6. AUDIO OUT-SOCKETS
7. DIGITAL OUT-SOCKET
8. REMOTE CONTROL

Controller

Frontpanel:

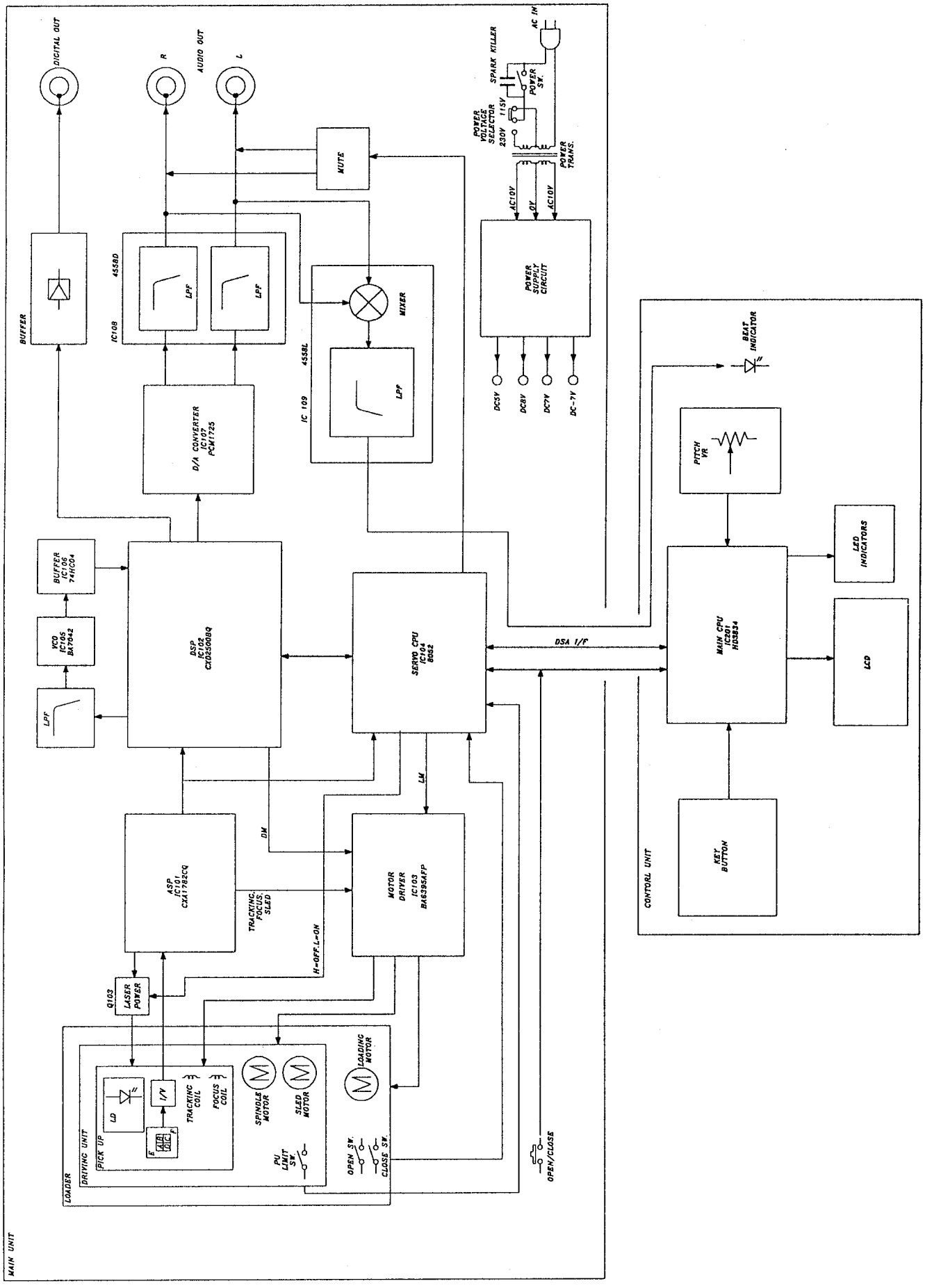


1. SECTION UNIT 1
2. SECTION UNIT 2
3. OPEN/CLOSE BUTTONS
4. DISPLAY
5. SHUTTLE-WHEEL
6. JOG-WHEEL
7. SKIP-BUTTONS
8. CUE-BUTTON
9. PLAY/PAUSE-BUTTON
10. LOOP-BUTTON
11. PITCH BEND-BUTTONS
12. PITCH-BUTTON
13. PITCHFADER
14. TIME-BUTTON
15. SINGLE-BUTTON
16. PROGRAM-BUTTON

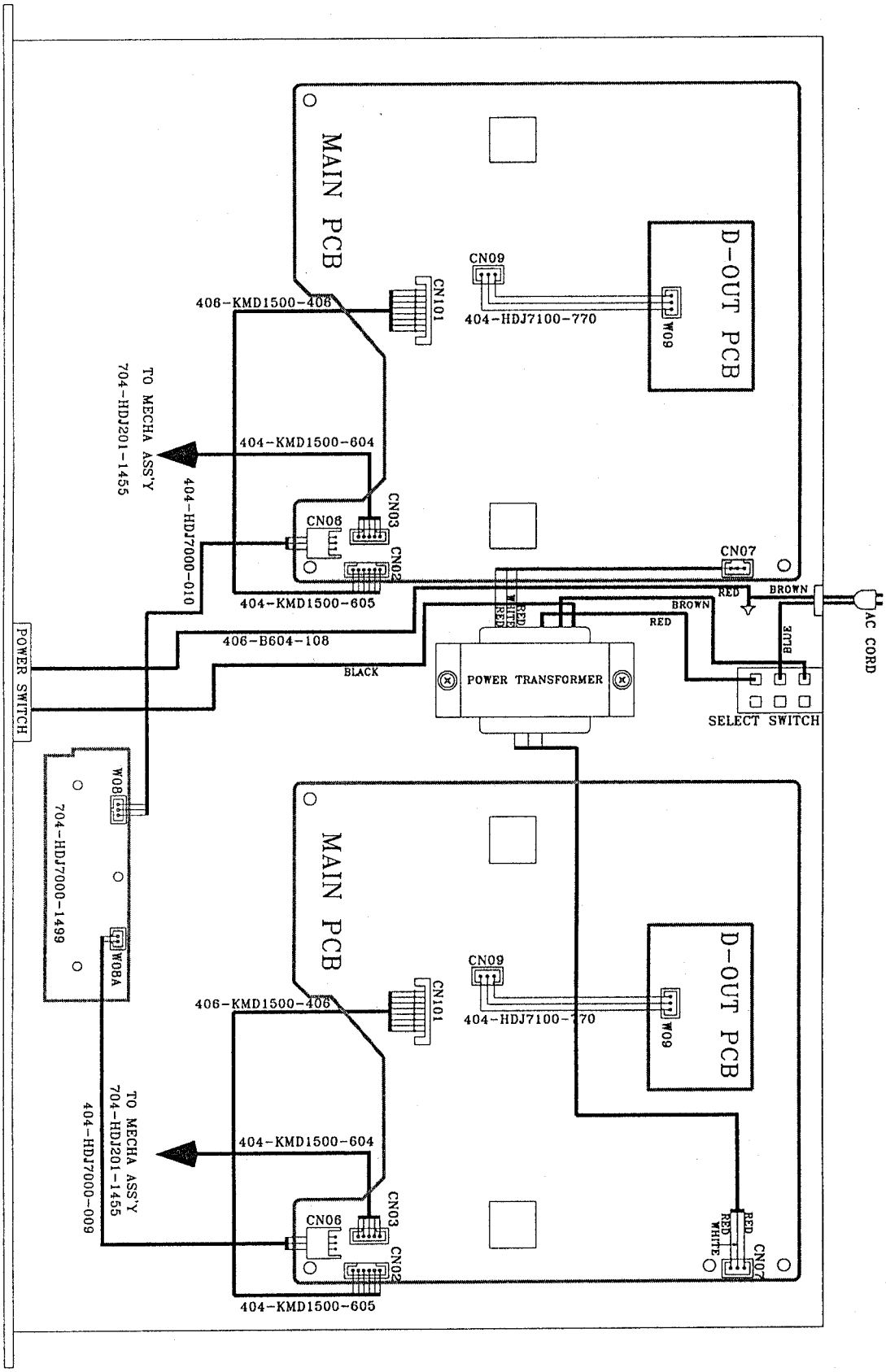
Rear panel:

17. CONNECTOR PORTS

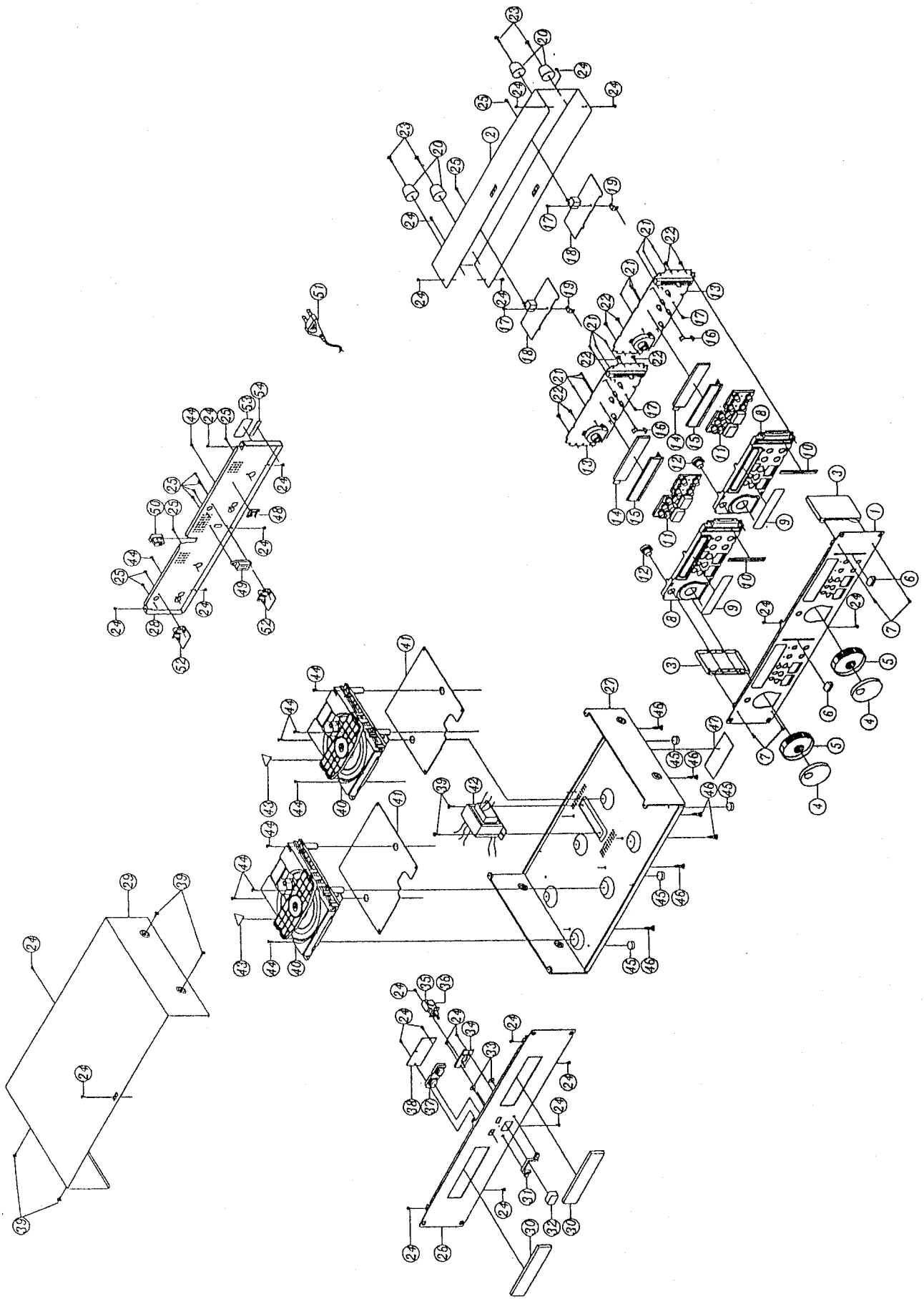
BLOCK DIAGRAM



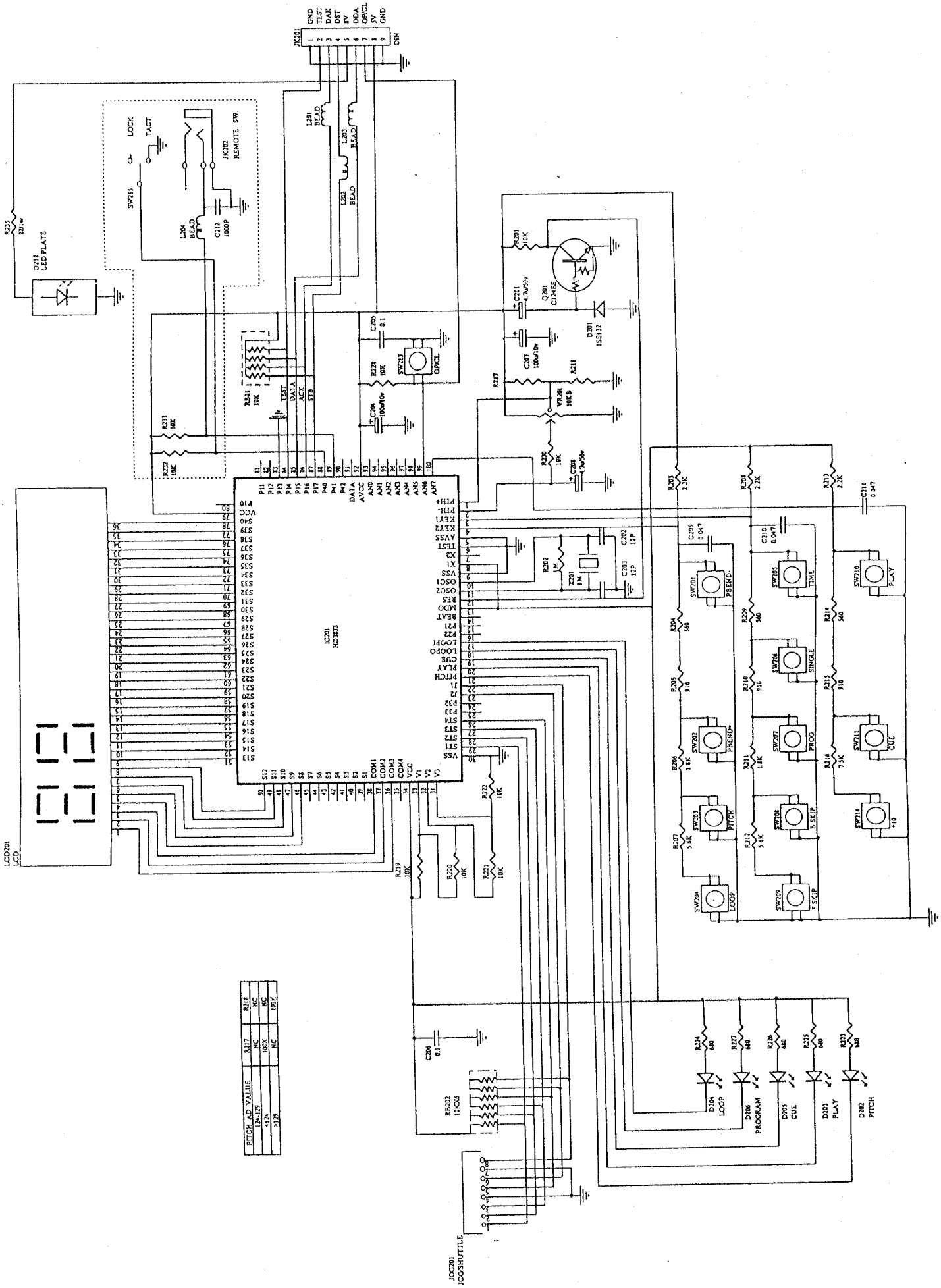
POINT-TO-POINT WIRING DIAGRAM



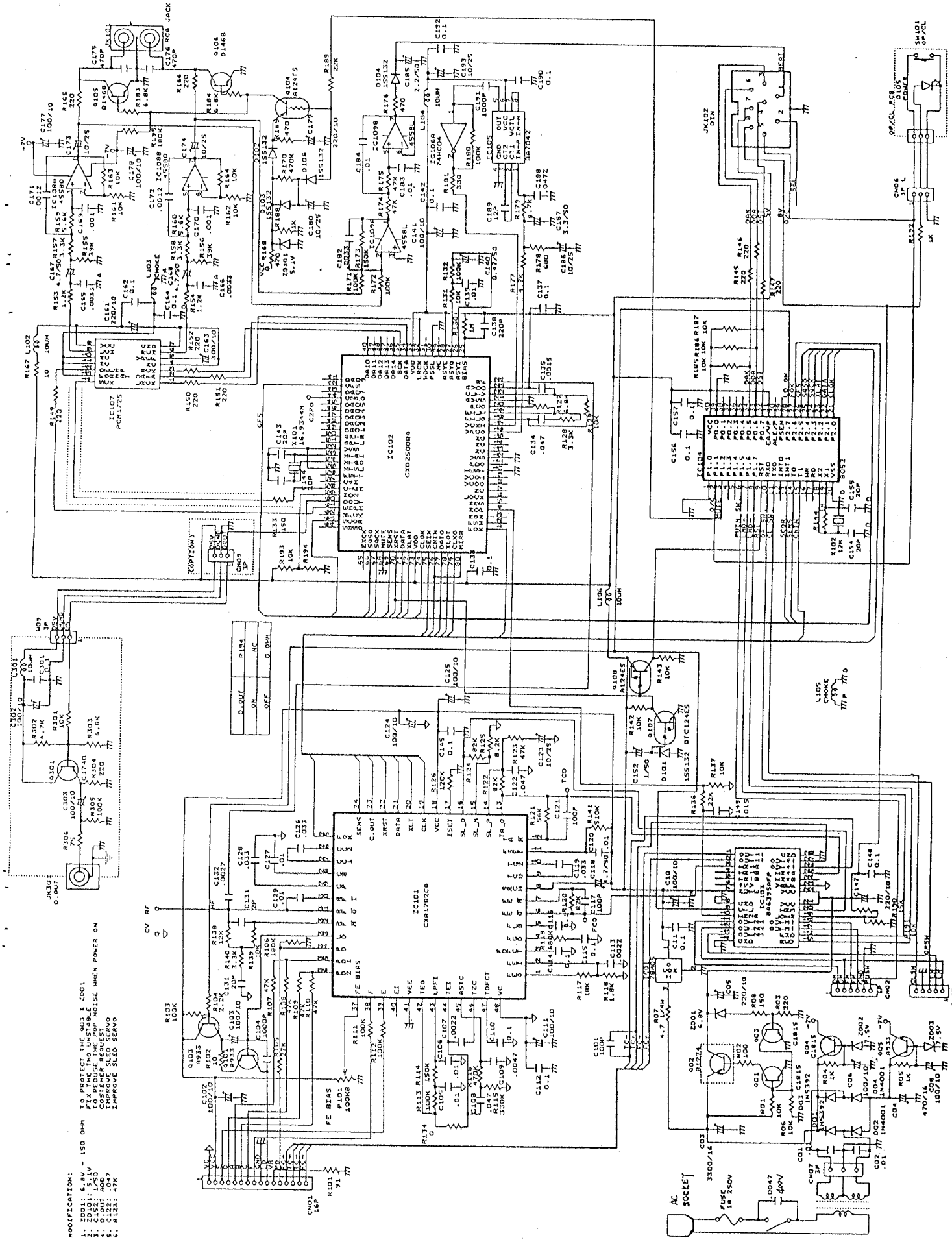
EXPLODED VIEW



SCHEMATIC DIAGRAM

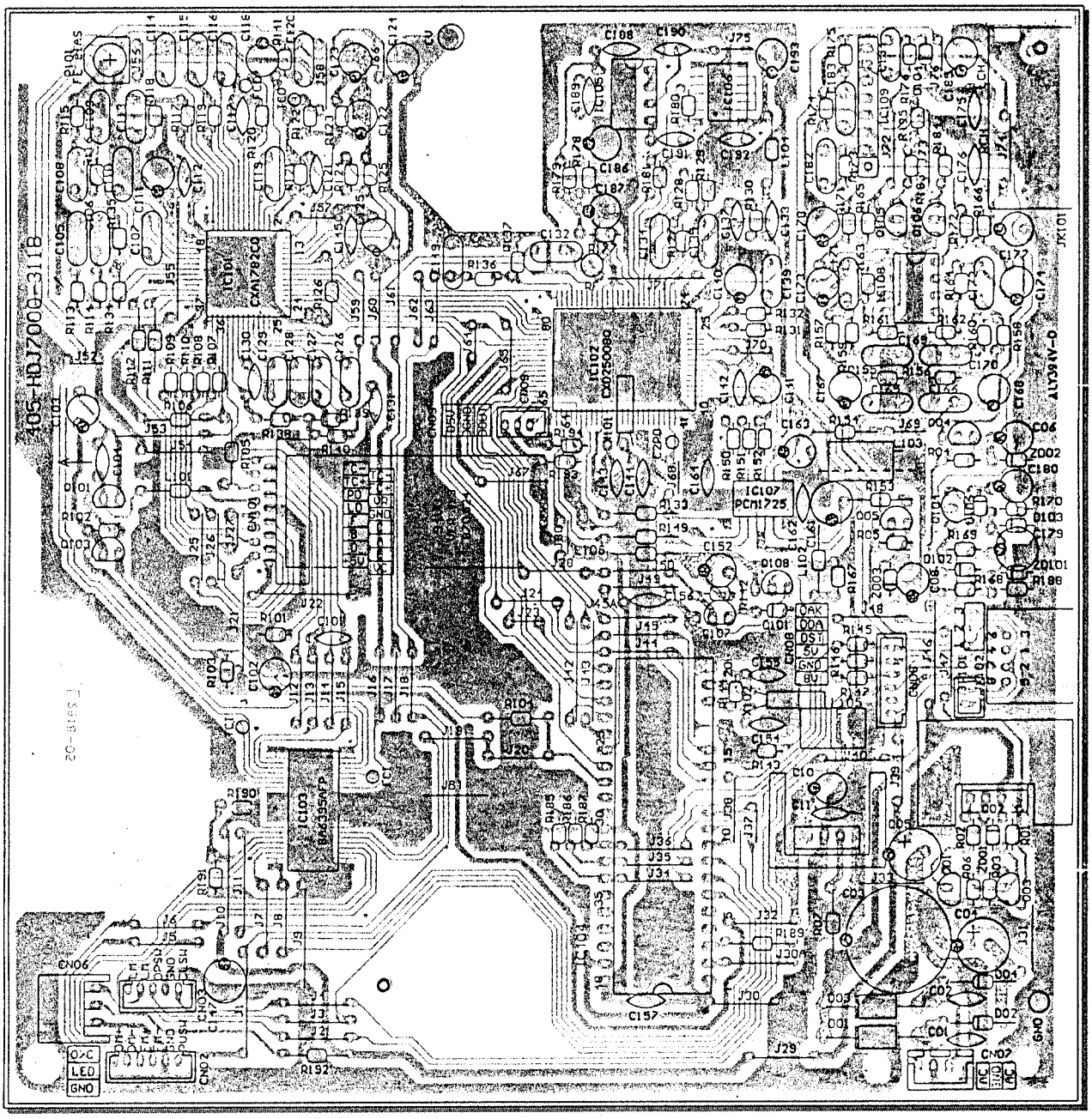


SCHEMATIC DIAGRAM



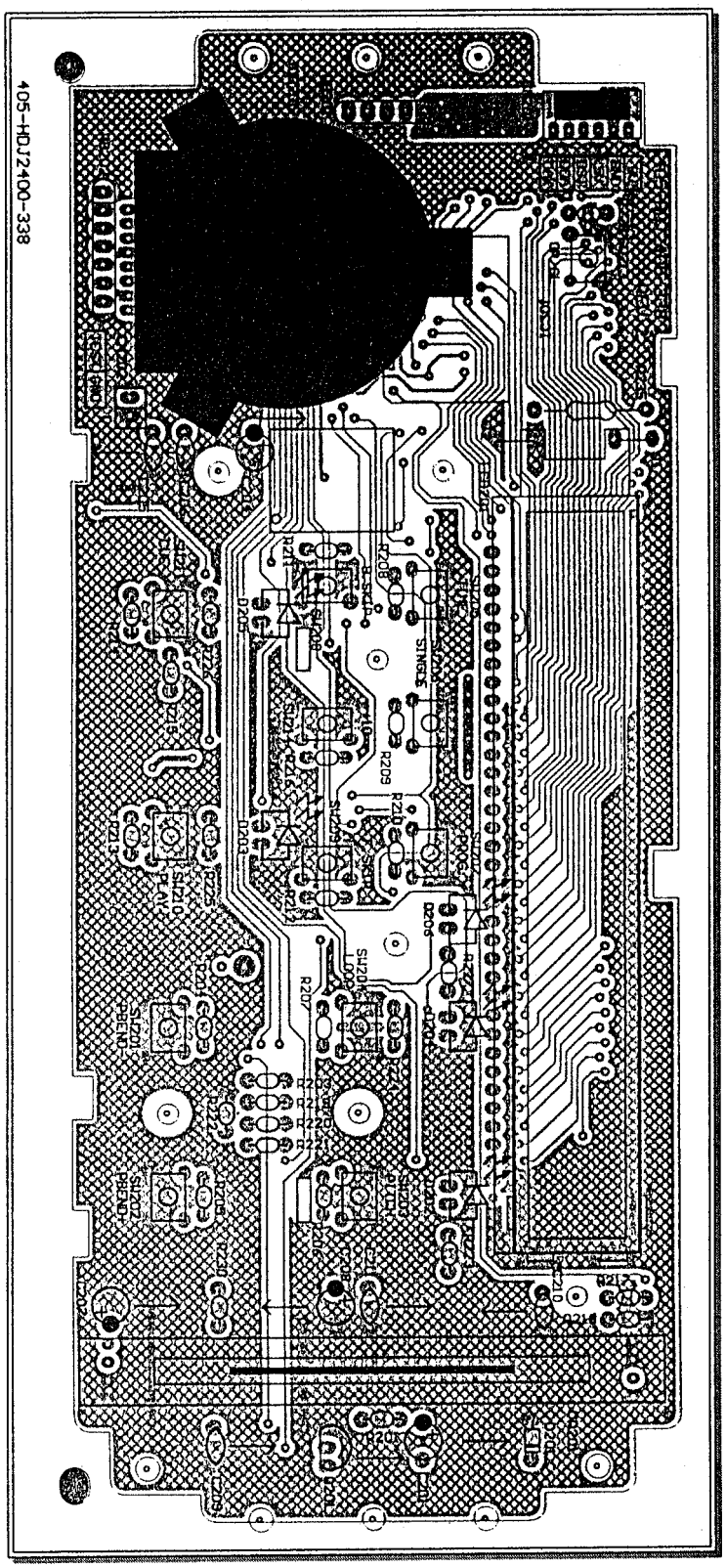
PRINTED CIRCUIT DIAGRAM

MAIN PCB



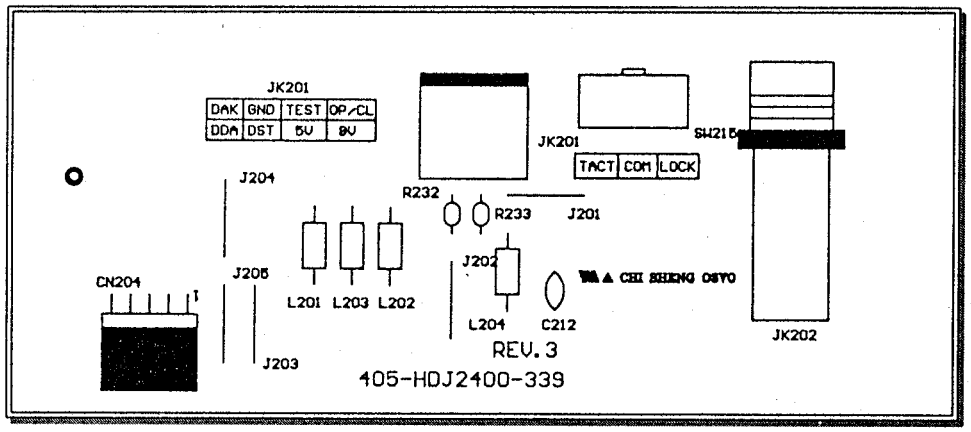
PRINTED CIRCUIT BOARD

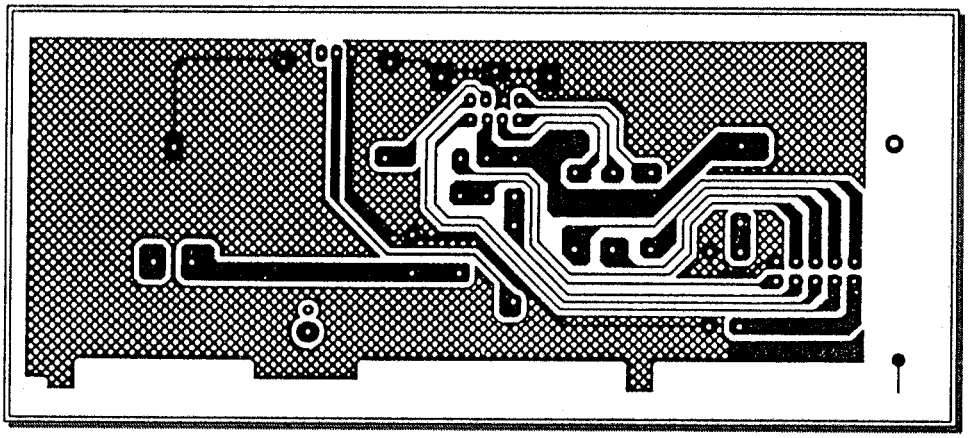
CONTROL PCB



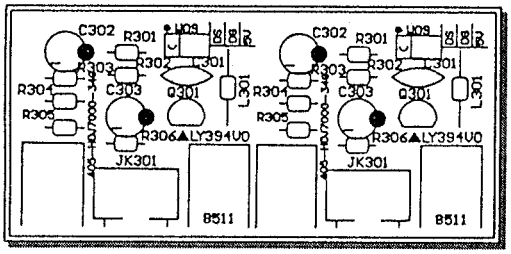
PRINTED CIRCUIT BOARD

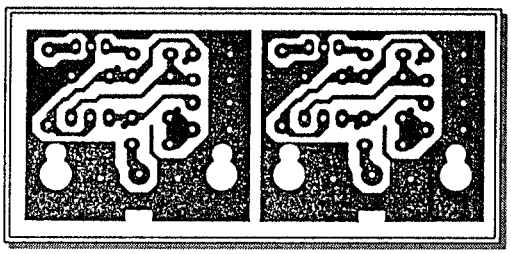
OUTPUT PCB



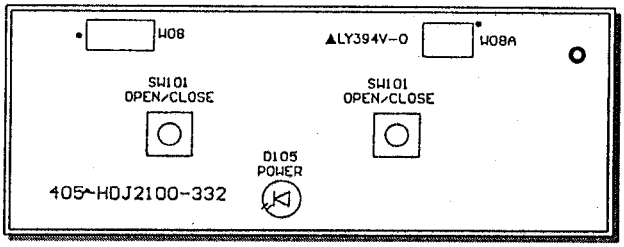


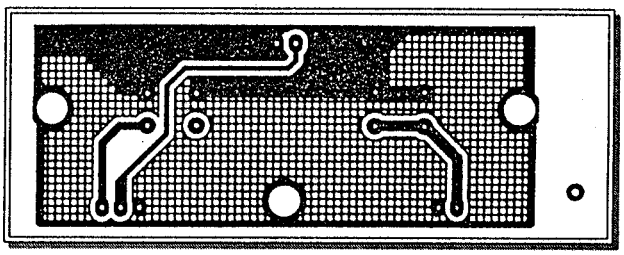
DIGITAL OUTPUT PCB





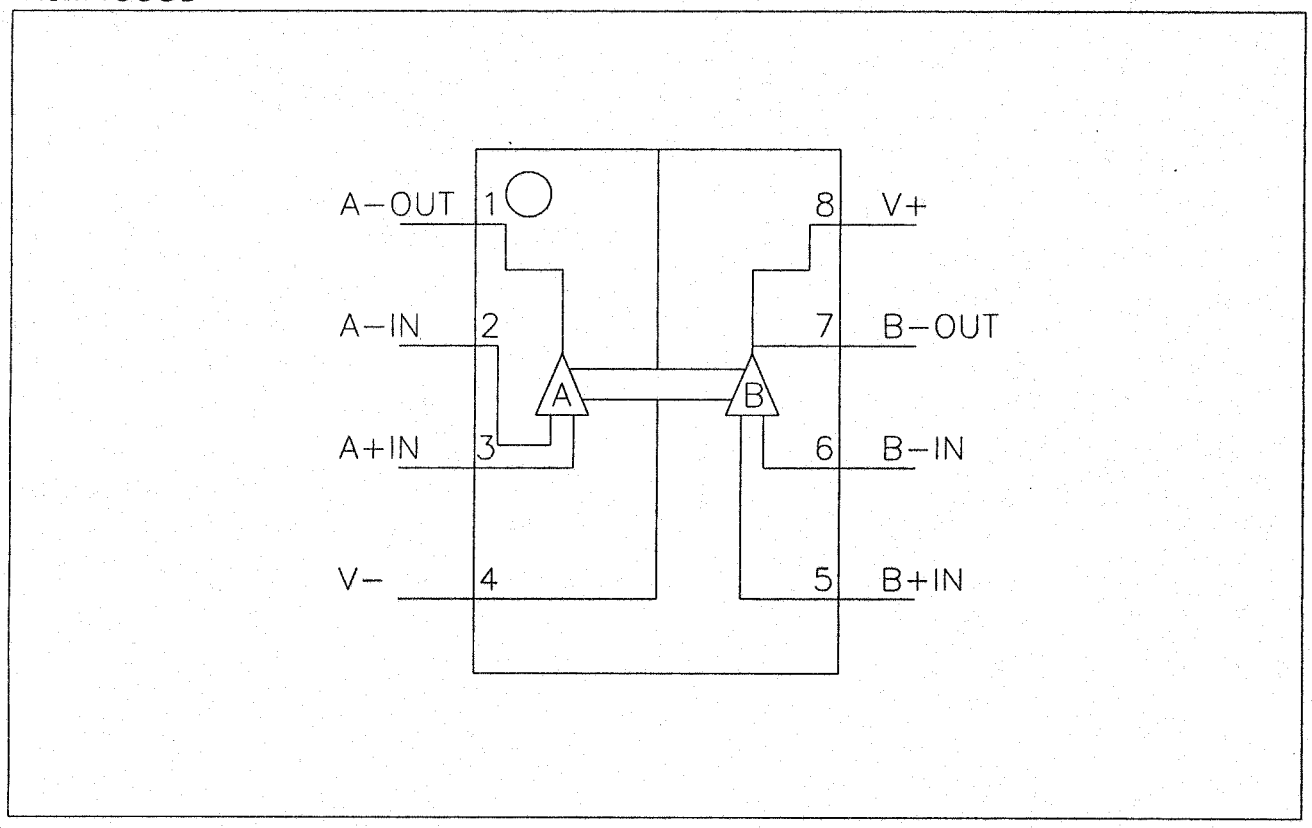
SWITCH PCB



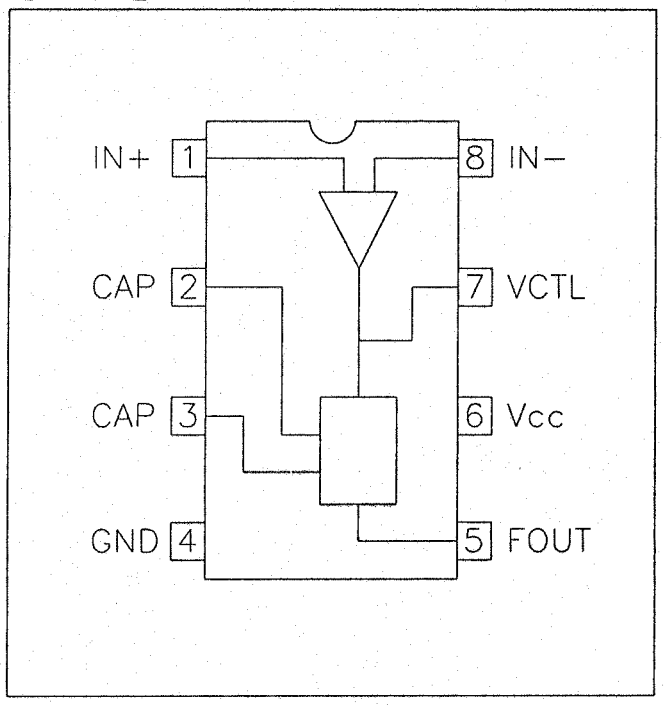


PRINTED CIRCUIT BOARD

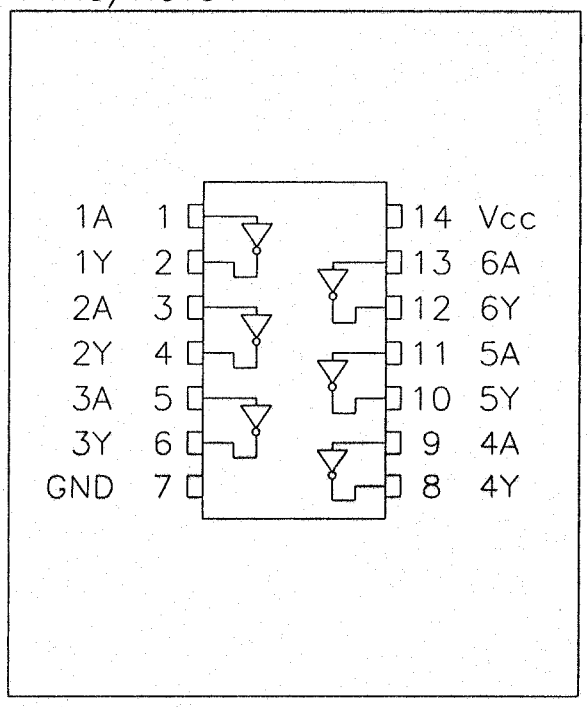
NJM4558D



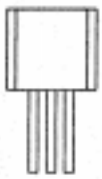
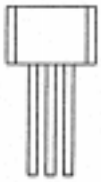
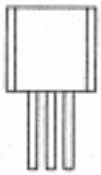
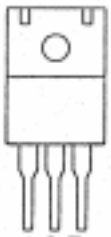
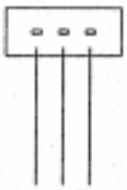
BA7042



74HC/HCT04



SEMICONDUCTOR LEAD IDENTIFICATION

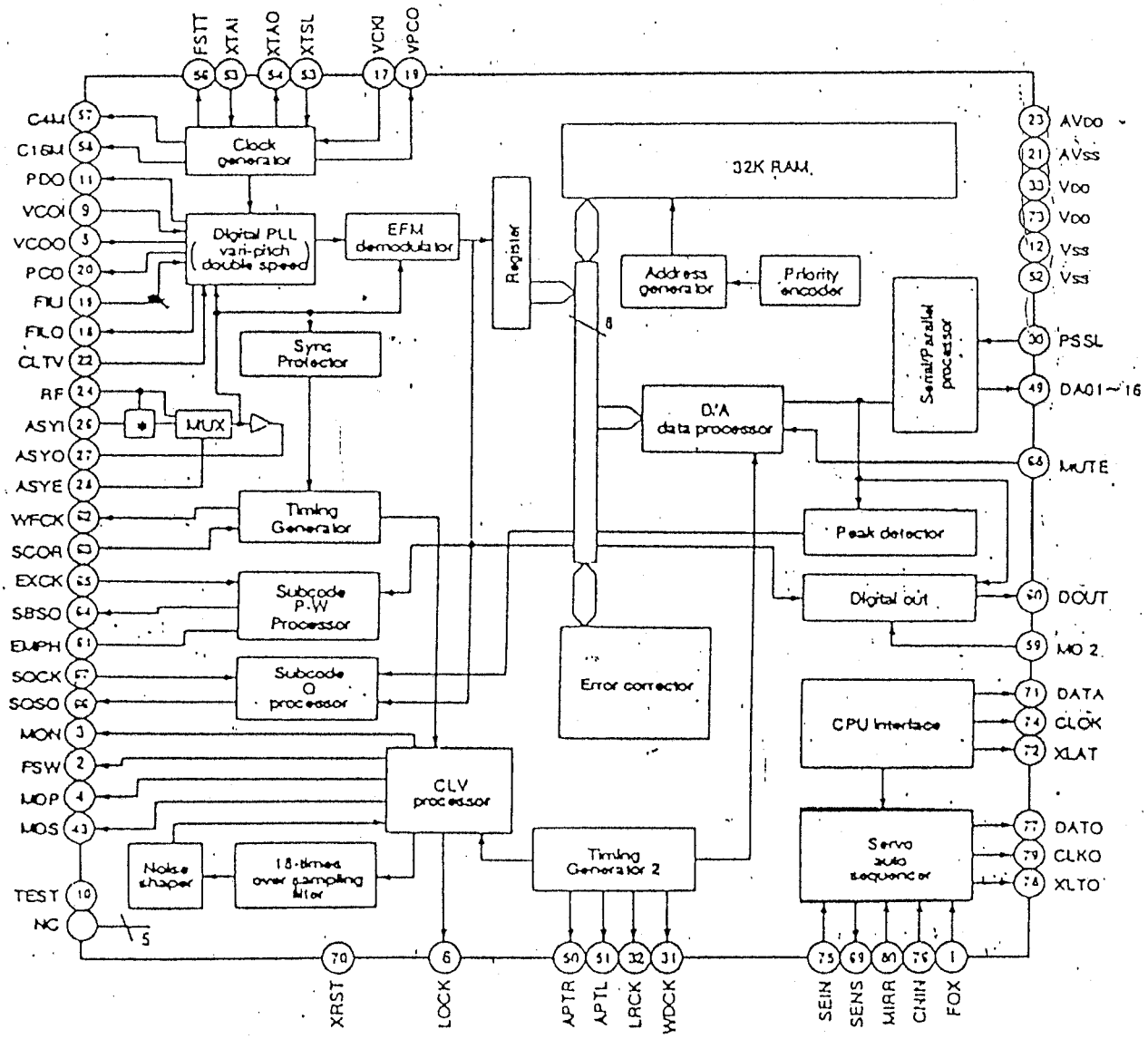
TRANSISTOR	FRONT VIEW	BOTTOM VIEW
B1010 D1384	 ECB	 ECB
A933 C1740 C124ES D1468 C124TS	 ECB	 ECB
79L06A	 213	 213
78M05A	 123	 123

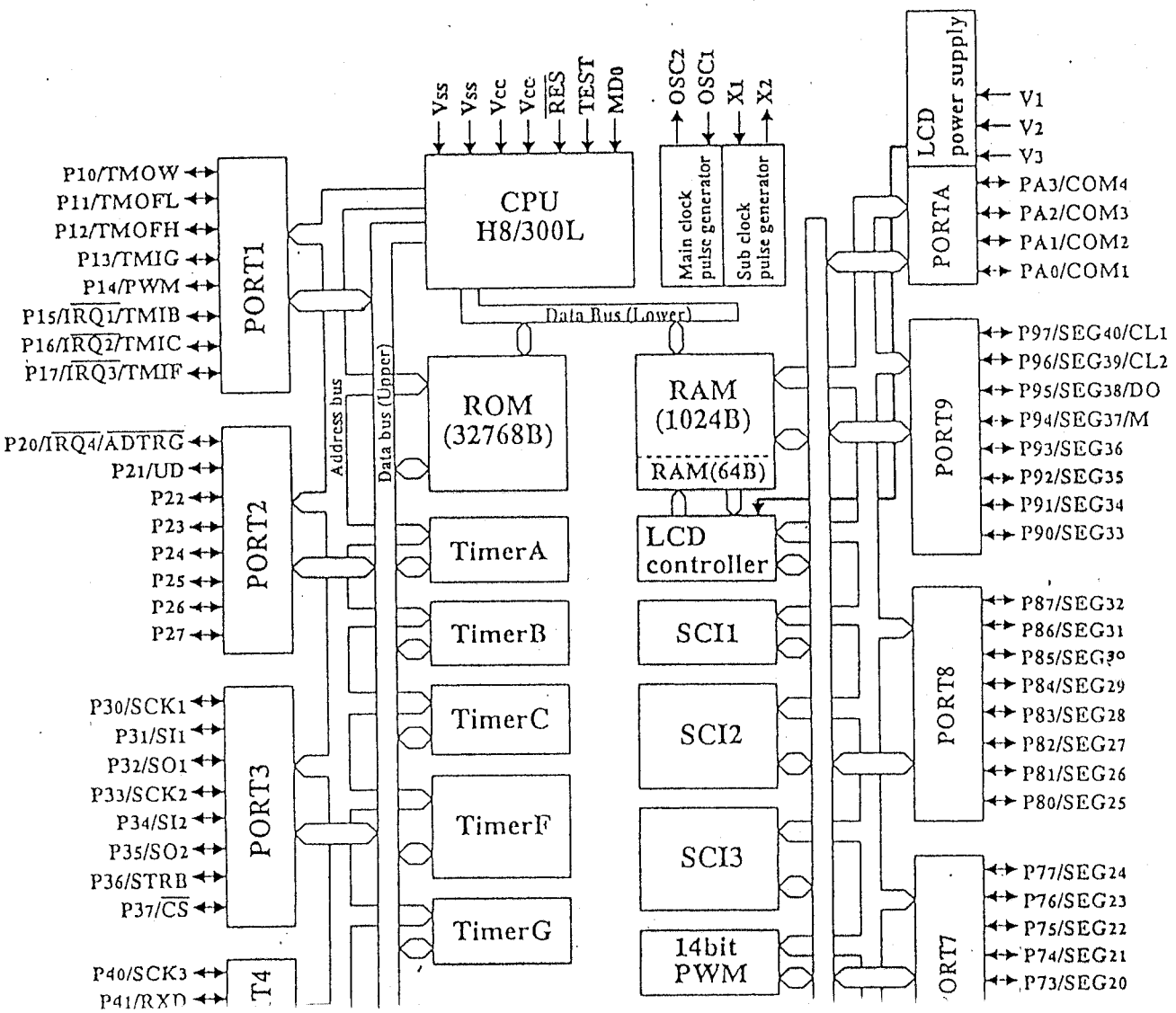
TERMINAL NAME

B → BASE
C → COLLECTOR
E → EMITTER

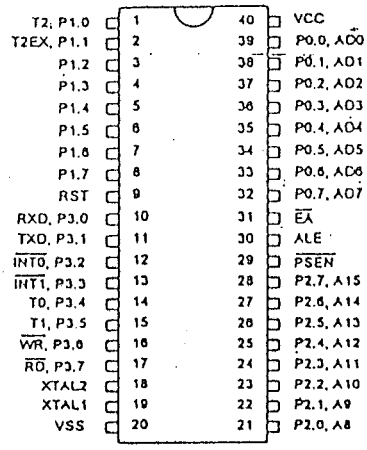
1 → INPUT
2 → GND
3 → OUTPUT

CXD2500BQ

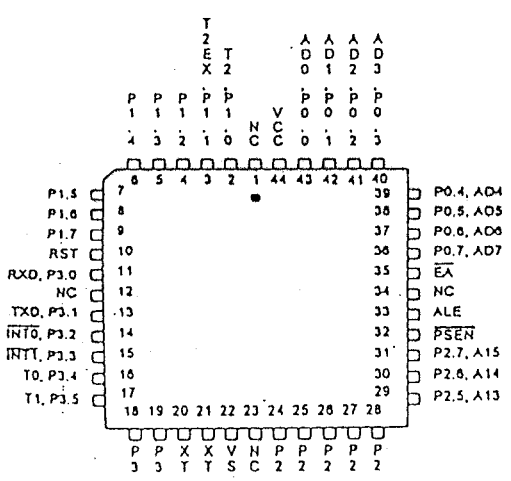

FSTT
XTAI
XTAO
XTSL
VCKI
VPCO
C4M
C16M
PDO
VCOI
VCOO
PCO
FILI
FILO
CLTV
RF
ASYI
ASYO
ASYE
WFCK
SCOR
EXCK
SBSO
EMPH
SOCK
SOSO
MON
FSW
MOP
MOS
TEST
NC
Clock generator
Digital PLL vari-pitch double speed
EFM demodulator
Sync Protector
MUX
Timing Generator
Subcode P-W Processor
Subcode Q processor
CLV processor
Noise shaper
18-times over sampling filter
Register
32K RAM
Address generator
Priority encoder
D/A data processor
Timing Generator 2
Error corrector
Peak detector
Digital out
CPU Interface
Servo auto sequencer
Serial/Parallel processor
AVDD
AVSS
VDD
VDD
VSS
VSS
PSSL
DA01~16
MUTE
DOUT
MD 2
DATA
CLOK
XLAT
DATO
CLKO
XLTO
XRST
LOCK
APTR
APTL
LRCK
WDCK
SEIN
SENS
MIRR
CHIN
FOK


Vss
Vss
Vcc
Vcc
RES
TEST
MD0
OSC2
OSC1
X1
X2
CPU
H8/300L
Main clock pulse generator
Sub clock pulse generator
LCD power supply
V1
V2
V3
PORTA
PA3/COM4
PA2/COM3
PA1/COM2
PA0/COM1
P10/TMOW
P11/TMOFL
P12/TMOFH
P13/TMIG
P14/PWM
P15/IRQ1/TMIB
P16/IRQ2/TMIC
P17/IRQ3/TMIF
PORT1
Address bus
Data bus (Upper)
Data Bus (Lower)
ROM
(32768B)
RAM
(1024B)
RAM(64B)
P20/IRQ4/ADTRG
P21/UD
P22
P23
P24
P25
P26
P27
PORT2
TimerA
LCD
controller
PORT9
P97/SEG40/CL1
P96/SEG39/CL2
P95/SEG38/DO
P94/SEG37/M
P93/SEG36
P92/SEG35
P91/SEG34
P90/SEG33
TimerB
SCI1
P30/SCK1
P31/SI1
P32/SO1
P33/SCK2
P34/SI2
P35/SO2
P36/STRB
P37/CS
PORT3
TimerC
SCI2
PORT8
P87/SEG32
P86/SEG31
P85/SEG30
P84/SEG29
P83/SEG28
P82/SEG27
P81/SEG26
P80/SEG25
TimerF
SCI3
TimerG
14bit
PWM
P40/SCK3
P41/RXD
T4
ORT7
P77/SEG24
P76/SEG23
P75/SEG22
P74/SEG21
P73/SEG20

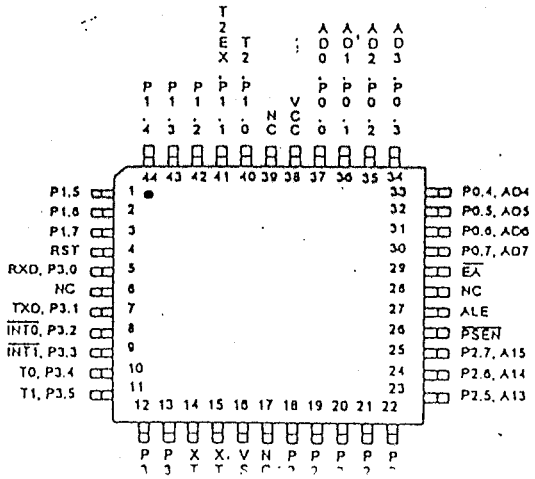
40-Pin DIP (W78C52C)

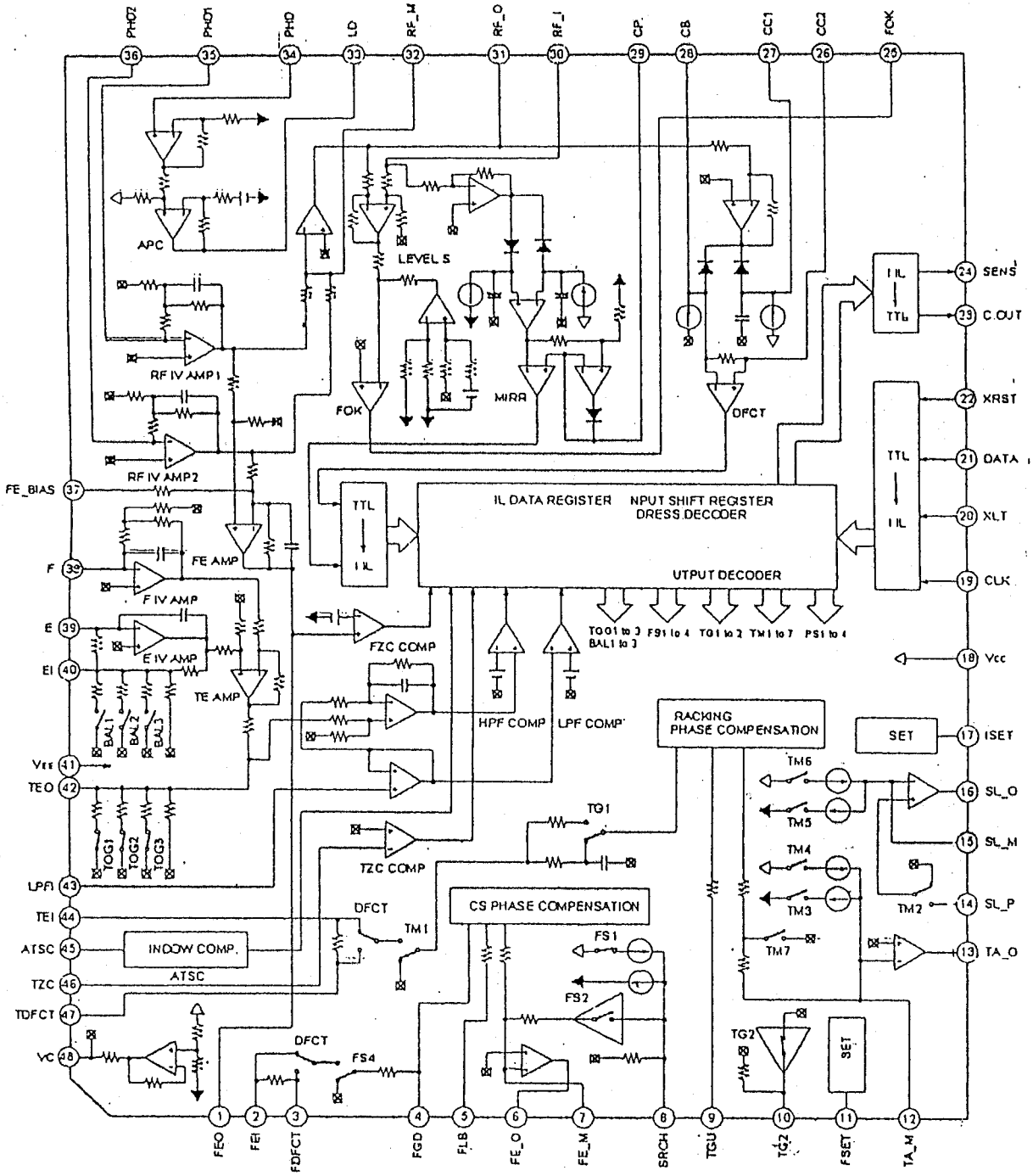


44-Pin PLCC (W78C52CP)



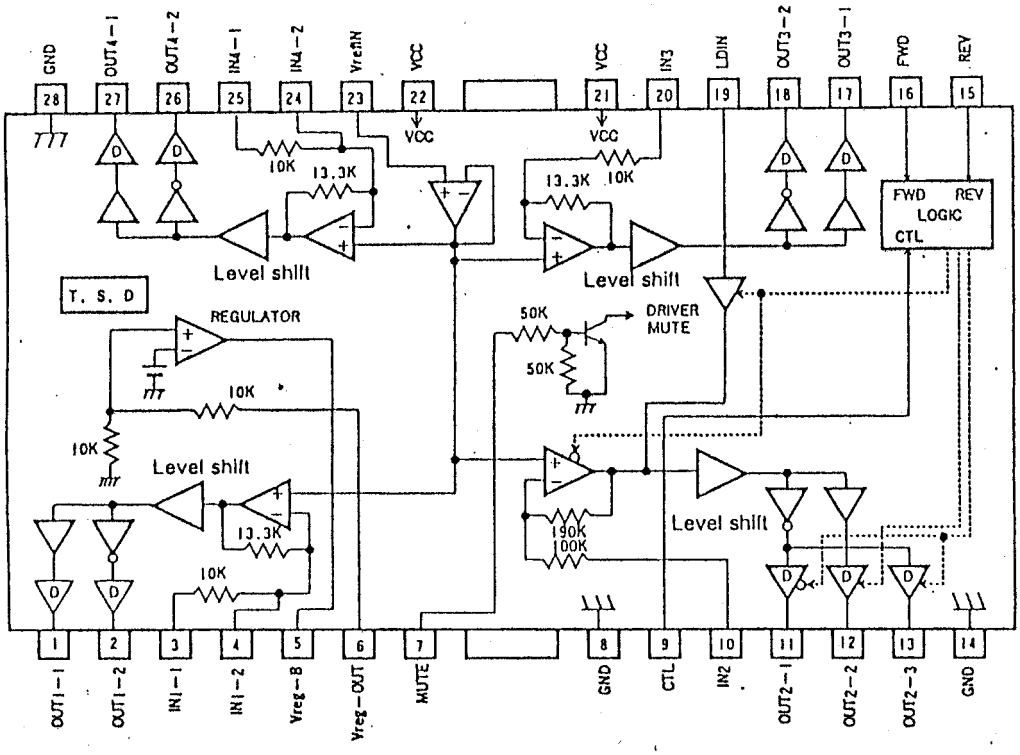
44-Pin QFP (W78C52CF)





- The switch state in Block Diagram is for initial resetting.
- Switch turns to ◦ side for 1 and to • side for 0 in Serial Data Truth Table.
- DFCT switch turns to ◦ side when defect signal generates for DEFECT = E in Serial Data Truth Table.
- TG1 switch turns to ◦ side and TG2 switch is left open when TG1 and TG2 (address 1 : D3) is 1.

BA6395AFP



1 Pin description (Sheet 1 of 2)

T.S.D. : Thermal shut down
D : Driver buffer
Units for resistance value : (Ω)